## AMENDMENT TO CLAIMS

Please **AMEND** claim 9 and cancel claims 1, 4 – 8, and 12 – 14 without prejudice or disclaimer. Applicants expressly reserve the right to refile the subject matter of these canceled claims in one or more continuation applications.

This listing of claims will replace all prior versions, and listings, of claims in the application:

### ***Listing of Claims***

Claims 1 – 8. (Canceled).

9. (Currently amended) A ~~The~~ semiconductor structure ~~of claim 8,~~ formed on a substrate, comprising:

an n-channel field effect transistor having a source, a drain, a gate, and a direction of current flow from the source to the drain; ~~and~~

a first shallow trench isolation for the n-channel field effect transistor comprising a first shallow trench isolation side, the first shallow trench isolation side having at least one overhang configured to prevent oxidation induced stress in a direction parallel to the direction of current flow for the n-channel field effect transistor,

the first shallow trench isolation for the n-channel field effect transistor further comprising a second shallow trench isolation side being transverse to the first shallow trench isolation side and having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the n-channel field effect transistor;

a p-channel field effect transistor, the p-channel field effect transistor having a source, a drain, a gate, and a direction of current flow from the source to the drain;

a second shallow trench isolation for the p-channel field effect transistor having a third shallow trench isolation side, the third shallow trench isolation side being devoid of an overhang; and

the second shallow trench isolation for the p-channel field effect transistor further having a fourth shallow trench isolation side, the fourth shallow trench isolation side being transverse to the third shallow trench isolation side and having at least one overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow for the p-channel field effect transistor.

10. (Original) The semiconductor structure of claim 9, wherein the overhang configured to prevent oxidation induced stress in a direction transverse to the direction of current flow prevents a degradation of hole mobility.

11. (Original) The semiconductor structure of claim 9, wherein:

the distance from the gate of the n-channel field effect transistor to the first shallow trench isolation side of the first shallow trench isolation for the n-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the first shallow trench isolation would affect performance of the n-channel field effect transistor, and

the distance from the gate of the n-channel field effect transistor to the second shallow trench isolation side of the first shallow trench isolation for the n-channel field

effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the second shallow trench isolation would affect performance of the n-channel field effect transistor.

Claims 12 - 14. (Canceled).

15. (Original) The semiconductor structure of claim 9, wherein the distance from the gate of the p-channel field effect transistor to the fourth shallow trench isolation side for the second shallow trench isolation for the p-channel field effect transistor is less than or equal to a distance within which oxidation induced stress adjacent to the fourth shallow trench isolation side would affect performance of the p-channel field effect transistor.

16. (Original) The semiconductor structure of claim 15, wherein the distance from the gate of the p-channel field effect transistor to the fourth shallow trench isolation side is less than or equal to about 5.0 microns.

17. (Original) The semiconductor structure of claim 11, wherein the distance from the gate of the n-channel field effect transistor to the first shallow trench isolation side is less than or equal to about 5.0 microns.

18. (Previously Presented) The semiconductor structure of claim 11, wherein the distance from the gate of the n-channel field effect transistor to the second shallow trench isolation side is less than or equal to about 5.0 microns.

Claims 19 – 22. (Canceled).